WHAT IS CLAIMED IS:

1. A method for fabricating vias, comprising:

placing at least one semiconductor wafer having at least one via adjacent to an interconnect onto a pedestal;

controlling the temperature of the interconnect to be less than the temperature at which the interconnect transits from a tensile to a compressive mode; and

depositing a coating lining the via.

2. The method of Claim 1 wherein the interconnect is selected from the group consisting of: aluminum, aluminum alloys, copper and copper alloys.

3. The method of Claim 1 wherein controlling the interconnect temperature comprises actively cooling the pedestal and using a low temperature depositing process.

4. The method of Claim 3 wherein actively cooling the pedestal comprises transferring heat to a medium flowing through the pedestal.

5. The method of Claim 4 wherein the flowing medium is water.

6. The method of Claim 4 wherein the flowing medium is liquid nitrogen.

7. The method of Claim 4 wherein the flowing medium is helium.

8. The method of Claim 1 wherein the coating is deposited by IMP.

9. The method of Claim 1 wherein the coating comprises two layers.

10. The method of Claim 9 wherein the two layers comprise an adhesion layer and a barrier layer.

11. The method of Claim 9 wherein the two layers are selected from the group consisting of one or more layers or combinations of: tantalum, tantalum nitride, tantalum silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride, titanium, and titanium nitride.

12. The method of Claim 1 wherein the coating comprises three layers.

13. The method of Claim 12 wherein the three layers comprise an adhesion layer, a barrier layer and a seeding layer.

14. The method of Claim 12 wherein the three layers are selected from the group consisting of one or more layers or combinations of: tantalum, tantalum nitride, tantalum silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride, titanium, titanium nitride, copper, and copper alloys.

15. The method of Claim 1 wherein the interconnect temperature no greater than about 100°C.

16. The method of Claim 1 wherein the interconnect temperature is controlled by decreasing the time for depositing the coating.

17. The method of Claim 16 wherein the time for depositing the coating is decreased by using a faster deposition rate.

18. The integrated circuit produced by the method of Claim 1 wherein interconnect extrusions in vias are eliminated.

19. A system for fabricating vias in an integrated circuit, comprising:

a pedestal having active cooling;

at least one semiconductor wafer on the pedestal, wherein the wafer comprises at least one via adjacent to an interconnect;

an ionized plasma generating tool; and

a source of material to form a coating lining the via;

wherein the system keeps the interconnect temperature below the temperature at which the interconnect transits from tensile to compressive stress thereby preventing interconnect extrusions in the via.

20. The system of Claim 19 wherein the interconnect is selected from the group consisting of: aluminum, aluminum alloys, copper and copper alloys.

21. The system of Claim 19 wherein the active cooling comprises transferring heat to a medium flowing through the pedestal.